

Claims

What is claimed is:

1 1. A testing circuit for tracking transistor stress degradation
2 comprising:

3 a first array of P-channel field effect transistors (PFETs) connected in
4 parallel; said first array of PFETs being stressed by applying a low gate input
5 and a high source and a high drain for the PFETs during a stress period; and
6 said first array of PFETs being tested by operating the PFETs in a saturated
7 region during a test period; and

8 a reference array of PFETs not being stressed during the stress
9 period and said reference array of PFETs being activated for testing to
10 compare a saturated drain current performance with said first array of
11 PFETs during the test period.

1 2. A testing circuit as recited in claim 1 includes a first current
2 source N-channel FET (NFET) device coupled to said first array of PFETs;
3 and a test signal input applied to a gate of said first current source NFET
4 device to activate said current source NFET device during the test period.

1 3. A testing circuit as recited in claim 2 includes a second current
2 source N-channel FET (NFET) device coupled to said reference array of
3 PFETs; and said test signal input applied to a gate of said second current
4 source NFET device to activate said current source NFET device for testing;
5 said first and said second NFET devices being substantially identical
6 devices.

1 4. A testing circuit as recited in claim 3 includes at least one
2 additional NFET device connected in parallel with said second current
3 source NFET device coupled to said reference array of PFETs; said at least
4 one additional NFET device for supplying a predetermined amount of
5 additional load current to reference array of PFETs.

1 5. A testing circuit as recited in claim 4 wherein said at least one
2 additional NFET device having a set width equal to a selected percent of a
3 width of said substantially identical first and said second NFET devices; said
4 set width of said at least one additional NFET device selectively provided to
5 identify a predefined level of degradation of said first array of PFETs.

1 6. A testing circuit as recited in claim 4 includes a reference
2 NFET device coupled between a respective source of each of said first and
3 said second current source NFET devices and said at least one additional
4 NFET device and ground for level shifting.

1 7. A testing circuit as recited in claim 4 includes a gated input
2 stage comparator coupled to said first array of PFETs and said reference
3 array of PFETs and receiving said test signal input to activate said gated
4 input stage comparator during the test period.

1 8. A testing circuit as recited in claim 7 wherein said gated input
2 stage comparator has a first input connected to drain connections of said
3 first array of PFETs and said first current source NFET device for
4 comparison with a second input connected to the drain connections said
5 reference array of PFETs and said second current source NFET device and
6 said at least one additional NFET device.

1 9. A testing circuit as recited in claim 1 wherein said first array of
2 PFETs is stressed by applying a continuous low gate input to the PFETs
3 during the stress period.

1 10. A testing circuit as recited in claim 1 wherein said first array of
2 PFETs is stressed by applying a dynamic low gate input to the PFETs
3 having a selected duty cycle during the stress period.

1 11. A testing circuit as recited in claim 10 wherein said dynamic
2 low gate input to the PFETs having a selected duty cycle during the stress
3 period is provided by an oscillator and combinational logic.

1 12. A method for tracking transistor stress degradation comprising
2 the steps of:
3 providing a first array of P-channel field effect transistors (PFETs)
4 connected in parallel;
5 applying a low gate input and a high source and a high drain for the
6 PFETs to stress said first array of PFETs during a stress period;
7 operating the PFETs in a saturated region to test said first array of
8 PFETs during a test period;
9 providing a reference array of PFETs not being stressed during the
10 stress period; and
11 activating said reference array of PFETs to compare a saturated drain
12 current performance with said first array of PFETs during the test period.

1 13. A method for tracking transistor stress degradation as recited
2 in claim 12 wherein the step of operating the PFETs in a saturated region to
3 test said first array of PFETs during a test period includes the steps of
4 coupling a first current source N-channel FET (NFET) device to said first
5 array of PFETs; and applying a test signal input to a gate of said first current
6 source NFET device to activate said current source NFET device during the
7 test period.

1 14. A method for tracking transistor stress degradation as recited
2 in claim 13 wherein the step of activating said reference array of PFETs to
3 compare a saturated drain current performance with said first array of
4 PFETs during the test period includes the steps of coupling a second current
5 source NFET device to said reference array of PFETs; and applying said test
6 signal input to a gate of said second current source NFET device to activate
7 said current source NFET device during the test period.

1 15. A method for tracking transistor stress degradation as recited
2 in claim 14 includes the steps of coupling at least one additional NFET
3 device to said reference array of PFETs for supplying a predetermined
4 amount of additional load current to reference array of PFETs during the test
5 period.

1 16. A method for tracking transistor stress degradation as recited
2 in claim 15 includes the steps of coupling a gated input stage comparator
3 coupled to said first array of PFETs and said reference array of PFETs; and
4 applying said test signal to activate said gated input stage comparator during
5 the test period.

1 17. A method for tracking transistor stress degradation as recited
2 in claim 12 wherein the step of applying a low gate input and a high source
3 and a high drain for the PFETs to stress said first array of PFETs during a
4 stress period includes the steps of applying a continuous low gate input to
5 the PFETs to stress said first array of PFETs during the stress period.

1 18. A method for tracking transistor stress degradation as recited
2 in claim 12 wherein the step of applying a low gate input and a high source
3 and a high drain for the PFETs to stress said first array of PFETs during a
4 stress period includes the steps of applying a dynamic low gate input to the
5 PFETs having a selected duty cycle to stress said first array of PFETs during
6 the stress period.